REMARKS

Claims 1, 3-11, 13-20 and 22-28 are pending in the instant application. Claims 1, 4, 5, 7, 8, 11, 14, 15, 18, 19, 20, 23, 24, 27 and 28 are amended. Claims 2, 3, 6, 12, 12, 17, 21, 22 and 26 are cancelled. Claims 1, 3-11, 13-20 and 22-28 are rejected. No new matter has been added by the aforementioned amendments.

Examiner Interview

Applicant wishes to thank the Examiner for the interview granted and conducted on May 30, 2007. The Examiner has agreed to provide a written summary of the interview.

102 Rejection

Claims 1, 9-11, 16 and 20 are rejected under 35 U.S.C. § 102(e) as being anticipated by Dye (U.S. Patent No. 6,173,381). The Applicant has reviewed the cited references and respectfully submits that the embodiments of the invention as are set forth in Claims 1, 9-11, 16 and 20 are neither anticipated nor rendered obvious by Dye in view of Davis et al.

The Examiner is respectfully directed to independent Claim 1 which is drawn to a controller chip. Claim 1 is presented below in its entirety for the Examiner's convenient reference.

> 1. A controller chip comprising:
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> a graphics engine operative to manage a memory, the graphics engine comprising an integral interface; and
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> a circular first in first out (FIFO) buffer coupled to the graphics engine, the circular FIFO buffer being accessible by a central processing unit (CPU) through the graphics engine, wherein the graphics engine receives commands from the CPU via the integral interface, and manages the circular FIFO buffer via

the integral interface and wherein all data transmittable to the circular FIFO buffer is transmitted via the integral interface and the effective size of the circular FIFO buffer as viewed by the CPU can be as large as the memory.

Independent Claims 11 and 20 contain limitations similar to those contained in Claim 1. Claims 9-10 depend from Claim 1 and Claim 16 depends from Claim 11 and recite additional limitations of the present claimed invention.

As mentioned above, Dye does not anticipate or render obvious the embodiments of the present claimed invention as set forth in Claims 1, 11 and 20. Dye is deficient as Dye does not teach or suggest each of the limitations of Claims 1, 11 and 20 as is required to anticipate or render obvious these Claims. In particular, Dye does not teach or suggest a controller chip comprising a graphics engine (that comprises an integral interface) and a circular first in first out (FIFO) buffer where "all data transmittable to the circular FIFO buffer is transmitted via the integral interface and the effective size of the circular FIFO buffer as viewed by the CPU can be as large as the memory" as is recited in Claim 1 (independent Claims 11 and 20 recite similar limitations).

Claims 1, 11 and 20 have been amended to specifically recite that "all data transmittable to the circular FIFO buffer is transmitted via the integral interface" and that "the effective size of the circular FIFO buffer as viewed by the CPU can be as large as the memory." Support for the newly added limitation can be found in Applicants' specification at page 8, lines 16-20 and in Figure 4 where it is clearly shown that all data that is received by FIFO buffer 306 is transmitted through integral interface 303. It is important to note that the newly added limitations specifically and clearly set forth both the component via which all data that is received by the circular FIFO buffer is transmitted and the effective size of the circular FIFO buffer. These limitations (along

with the others recited in the Claims) must be taught or suggested by the cited combination in order for a proper prima facie case for rejection to be made.

Applicant respectfully submits that the newly added limitations are not taught or suggested anywhere in the Dye reference. However, if a rejection based on the Dye reference is maintained, Applicant respectfully requests that the location in the references where such is taught or suggested be clearly identified.

It should be appreciated that in order to anticipate or render obvious the embodiment of the invention that is set forth in Claim 1 (Claims 11 and 20 recite limitations similar to those recited in Claim 1) the Dye must teach or suggest, either expressly or inherently, in addition to all of the other limitations of Claim 1, a circular FIFO buffer and a graphics engine where: (1) the graphics engine includes an integral interface, (2) all data transmittable to the circular FIFO buffer is transmitted via the integral interface, and (3) the circular FIFO buffer as viewed by the CPU can be as large as the memory. Applicant respectfully submits that such a system structure and operation is not taught or suggested by Dye.

In the outstanding Office Action, it is contended that because Dye discloses that some data is transmittable to FIFO devices 214 and 216 from interface logic 202, the aforementioned limitations of Claim 1 are met. Applicant respectfully disagrees as Dye clearly does not teach or suggest that all of the data that is transmittable to any of the therein disclosed FIFO devices is transmitted via interface logic 202. As is clearly shown in Figure 5 of Dye, FIFO devices 214 and 216 receive inputs from not only interface logic 202 but from execution engine 210. Moreover, FIFO devices 214 and 216 receive inputs from both graphics engine 212 and memory controller 221. Importantly, as the disclosed FIFO devices of Dye receive data via components other than interface logic 202, the components equated to the recited integral interface and the

recited FIFO buffer of Claim 1 are clearly distinct therefrom. Accordingly, the arguments made with respect to these limitations are not supported by subject matter disclosed by Dye.

Dye discloses a memory controller that includes embedded data compression and decompression engines and uses data compression to reduce system bottlenecks. However, the system structure that is disclosed by Dye is distinct from that of the system that is set forth in the Applicant's Claims. Importantly, Dye does not show a controller graphics engine that includes an integral interface where all the data that is transmittable to a coupled circular FIFO buffer is transmitted via the integral interface as is set forth in Claim 1 (independent Claims 11 and 20 contain similar limitations). Consequently, Dye does not anticipate or render obvious the embodiment of the present claimed invention as is recited in Claim 1.

Because of the above outlined deficiencies, Applicant respectfully submit that Dye does not provide an adequate basis for rejection of Claims 1, 11 and 20 under 35 U.S.C. §102 and, as such, Claims 1, 11 and 20 are allowable. Accordingly, the Applicants respectfully submit that Claims 9-10 and 16 dependent on Claims 1 and 11 respectively are likewise allowable as being dependent on allowable base claims.

103 Rejection

Claims 3-8, 13-15, 17-19 and 22-28 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Dye (U.S. Patent No. 6,173,381) in view of Davis et al. (U.S. Patent No. 4,991,169). The Applicant has reviewed the cited references and respectfully submits that embodiments of the present claimed invention as are set forth in Claims 3-8, 13-15, 17-20 and 22-28 are neither anticipated nor rendered obvious by Dye in view of Davis et al.

The Examiner is respectfully directed to independent Claim 1 from which rejected Claims 3-8 depend and which recites limitations similar to those recited in independent Claims 11 and 20 from which rejected Claims 13-15 and 17-19 and rejected Claims 22-28 respectively depend. Claim 1 is presented below in its entirety for the Examiner's convenient reference.

> 1. A controller chip comprising:
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> a graphics engine operative to manage a memory, the graphics engine comprising an integral interface; and
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> a circular first in first out (FIFO) buffer coupled to the graphics engine,
>
> the circular FIFO buffer being accessible by a central processing unit (CPU) through the graphics engine, wherein the graphics engine receives commands from the CPU via the integral interface, and manages the circular FIFO buffer via the integral interface and wherein all data transmittable to the circular FIFO buffer is transmitted via the integral interface and the effective size of the circular FIFO buffer as viewed by the CPU can be as large as the memory.

Dye in view of Davis et al. does not anticipate or render obvious the embodiments of the present claimed invention as set forth in Claims 3-8, 13-15, 17-20 and 22-28. Dye in view of Davis et al. is deficient as Dye in view of Davis et al. does not teach or suggest each of the limitations of these Claims as is required to anticipate or render them obvious. In particular, Dye does not teach or suggest a controller chip comprising a graphics engine (that comprises an integral interface) and a circular first in first out (FIFO) buffer where "all data transmittable to the circular FIFO buffer is transmitted via the integral interface and the effective size of the circular FIFO buffer as viewed by the CPU can be as large as the memory" as is recited in Claim 1 as (from which, as alluded to above, rejected Claims 3-8 depend and which recites limitations similar to those recited in independent Claims 11 and 20 from which rejected Claims 13-15 and

17-19 and rejected Claims 22-28 respectively depend). And, Davis does not teach these limitations to remedy the deficiencies of Dye.

Davis et al. only shows a dual digital signal processor that provides real time links between multiple time division channels of a digital carrier signal. It should be appreciated that Davis et al. is concerned with providing a system that has the capacity to mediate communications between a carrier and a host system. However, nowhere in the Davis et al. reference is there shown a controller chip comprising a graphics engine (that comprises an integral interface) and a circular first in first out (FIFO) buffer where "all data transmittable to the circular FIFO buffer is transmitted via the integral interface and the effective size of the circular FIFO buffer as viewed by the CPU can be as large as the memory" as is recited in Claim 1 (from which rejected Claims 3-8 depend, and which recites limitations similar to those recited in independent Claims 11 and 20 from which rejected Claims 13-15 and 17-19 and rejected Claims 22-28 respectively depend).

Dye in view of Davis does not teach or suggest a controller chip comprising a graphics engine (that comprises an integral interface) and a circular first in first out (FIFO) buffer that includes limitations of Claim 1 discussed above and that further includes the limitation "in which the circular FIFO buffer comprises a double buffer" as is set forth in dependent Claim 4. Moreover, Applicant respectfully submits that Dye in view of Davis et al. does not teach or suggest a controller chip comprising a graphics engine (that comprises an integral interface) and a first in first out (FIFO) buffer that includes the above discussed limitations of Claim 1 and further includes the limitation "in which the circular FIFO buffer comprises a triple buffer" as is set forth in dependent Claim 5.

Applicant respectfully submits that Dye in view of Davis et al. does not teach or suggest a controller chip comprising a graphics engine (that comprises an integral interface) and a circular

first in first out (FIFO) buffer that includes the above discussed limitations of Claim 1 and further includes "a checking mechanism for determining if the circular FIFO buffer needs to be emptied without utilizing the CPU" as is set forth in dependent Claim 7. Moreover, Applicant respectfully submits that Dye in view of Davis et al. does not teach or suggest a controller chip comprising a graphics engine (that comprises an integral interface) and a circular first in first out (FIFO) buffer that includes the above discussed limitations of Claim 1 and further includes a checking mechanism that comprises: means for calculating the time required to fill the circular FIFO buffer; means for determining if the used memory of the circular FIFO buffer, is below a predetermined amount based upon the time required to fill the circular FIFO buffer; and means for preventing the circular FIFO buffer from filling if the used memory in the circular FIFO buffer is over the predetermined amount as is set forth in dependent Claim 8. Claims 13-15 and 17-19 dependent on Claim 11 and Claims 22-28 dependent on Claim 20 recite limitations similar to those recited in Claims 3-8 and are allowable for similar reasons.

For the reasons outlined above, Applicant respectfully submits that Dye in view of Davis et al. does not anticipate or render obvious the embodiments of the present claimed invention as are set forth in Claims 3-8 dependent on Claim 1, Claims 13-15 and 17-19 dependent on Claim 11 and Claims 22-28 dependent on Claim 20. Accordingly, Claims 3-8, 13-15 and 17-19 and 22-28 are allowable as they are dependent on allowable base Claims and as they recite additional limitations not taught or suggested by Dye in view of Davis et al.

Conclusion

In light of the above-listed remarks, the Applicant respectfully requests allowance of the remaining Claims.

The Examiner is urged to contact the Applicant's undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Respectfully submitted,

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